Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Withdrawn) A method of manufacturing an insulated-gate semiconductor device having an SOI structure, said method comprising the steps of:

forming a crystalline semiconductor on an insulative substrate or an insulating layer;

forming a source region, a drain region and a channel forming region by using the crystalline semiconductor;

forming impurity regions artificially and locally in the channel forming region so that said channel forming region includes carrier moving regions and said impurity regions,

wherein said impurity regions are added with an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed; and

forming a gate insulating film and a gate electrode on the channel forming region.

2. (Withdrawn) A method of manufacturing an insulated-gate semiconductor device having an SOI structure, said method comprising the steps of:

forming a crystalline semiconductor on an insulative substrate or an insulating layer;

forming a source region, a drain region and a channel forming region by using the crystalline semiconductor;

forming impurity regions artificially and locally in the channel forming region so that the channel forming region includes carrier moving regions and the impurity regions wherein said impurity regions are added with an impurity element for shifting an energy band in such a direction that movement of holes is obstructed; and

forming a gate insulating film and a gate electrode on the channel forming region.

3. (Withdrawn) A method according to claim 1 or 2 wherein said impurity element is for forming a built-in potential difference locally in the channel forming region.

4. (Withdrawn) A method according to claim 1 wherein said impurity element belongs to group XIII.

5. (Withdrawn) A method according to claim 4 wherein said impurity element is boron.

6. (Withdrawn) A method according to claim 2 wherein said impurity element belongs to group XV.

7. (Withdrawn) A method according to claim 6 wherein said impurity element is phosphorus or arsenic.

8. (Withdrawn) A method according to claim 1 or 2 wherein said carrier moving regions are intrinsic or substantially intrinsic.

9. (Withdrawn) A method according to claim 8 wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $2 \times 10^{18}$ atoms/cm$^3$.

10. (Withdrawn) A method according to claim 8 wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $1 \times 10^{17}$ atoms/cm$^3$.

11. (Withdrawn) A method according to claim 1 or 2 wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

12. (Withdrawn) A method according to claim 1 or 2 wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

13. (Withdrawn) A method according to claim 1 or 2 wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

14. (Withdrawn) A method according to claim 1 or 2 wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

15. (Withdrawn) A method according to claim 1 or 2 wherein said impurity regions have dot patterns.

16. (Withdrawn) A method according to claim 1 or 2 wherein said impurity regions have linear patterns substantially parallel with a channel direction.

17. (Withdrawn) A method according to claim 1 or 2 wherein said impurity element in said impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

18. (Previously Presented) An integrated circuit comprising:

a CMOS circuit;

an n-channel field effect transistor and a p-channel field effect transistor in the CMOS circuit;

said n-channel field effect transistor comprising:

a crystalline semiconductor formed on an insulating surface;

a source region, a drain region and a channel forming region in the crystalline semiconductor;

a gate insulating film;

a gate electrode formed over the channel forming region;

said channel forming region comprising:

a plurality of carrier moving regions;

a plurality of impurity regions,

wherein the plurality of impurity region of the channel forming region are formed locally for pinning of a depletion layer,

wherein the depletion layer is formed from the drain region toward the channel forming region and the source region,

wherein each of the impurity regions comprises an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

19. (Previously Presented) An integrated circuit comprising:

a memory circuit;

a field effect transistor in the memory circuit;

said field effect transistor comprising:

a crystalline semiconductor;

a source region, a drain region and a channel forming region in the crystalline semiconductor;

a gate insulating film;

a gate electrode formed over the channel forming region;

said channel forming region comprising:

a plurality of carrier moving regions;

a plurality of impurity regions;

wherein the plurality of the impurity region in the channel forming region are formed locally for pinning of a depletion layer,

wherein the depletion layer is formed from the drain region toward the channel forming region and the source region,

wherein each of the impurity regions comprises an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

20. (Previously Presented) An integrated circuit according to claim 18, wherein the impurity element is for forming a built-in potential difference locally in the channel forming region.

21. (Original) An integrated circuit according to claim 19, wherein said impurity element belongs to group XIII.

22. (Original) An integrated circuit according to claim 21, wherein said impurity element is boron.

23. (Previously Presented) An integrated circuit according to claim 18, wherein the impurity element belongs to group XV.

24. (Original) An integrated circuit according to claim 23, wherein said impurity element is phosphorus or arsenic.

25. (Previously Presented) An integrated circuit according to claim 18, wherein the carrier moving regions are intrinsic or substantially intrinsic.

26. (Original) An integrated circuit according to claim 25, wherein said substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $2 \times 10^{18}$ atoms/cm$^3$.

27. (Original) An integrated circuit according to claim 25, wherein said substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $1 \times 10^{17}$ atoms/cm$^3$.

28. (Previously Presented) An integrated circuit according to claim 18, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

29. (Previously Presented) An integrated circuit according to claim 18, wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

30. (Previously Presented) An integrated circuit according to claim 18, wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

31. (Previously Presented) An integrated circuit according to claim 18, wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

32. (Previously Presented) An integrated circuit according to claim 18, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

33. (Previously Presented) An integrated circuit according to claim 18, wherein the impurity regions have dot patterns.

34. (Previously Presented) An integrated circuit according to claim 18, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

35. (Previously Presented) An integrated circuit according to claim 18, wherein a threshold voltage is controlled by controlling widths of the carrier moving regions.

36. (Previously Presented) An integrated circuit according to claim 18, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

37. (Previously Presented) The integrated circuit of claim 18 in combination with at least an electric apparatus selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

38. (Withdrawn) A method according to claim 1, wherein said device is an EL display device.

39. (Original) An EL device having the integrated circuit according to claim 18.

40. (Original) An EL device having the integrated circuit according to claim 19.

41. (Previously Presented) An integrated circuit according to claim 19, wherein the impurity element is for forming a built-in potential difference locally in the channel forming region.

42. (Previously Presented) An integrated circuit according to claim 19, wherein the impurity element belongs to group XV.

43. (Previously Presented) An integrated circuit according to claim 42, wherein the impurity element is phosphorus or arsenic.

44. (Previously Presented) An integrated circuit according to claim 19, wherein the carrier moving regions are intrinsic or substantially intrinsic.

45. (Previously Presented) An integrated circuit according to claim 44, wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $2 \times 10^{18}$ atoms/cm$^3$.

46. (Previously Presented) An integrated circuit according to claim 44, wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $1 \times 10^{17}$ atoms/cm$^3$.

47. (Previously Presented) An integrated circuit according to claim 19, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

48. (Previously Presented) An integrated circuit according to claim 19, wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

49. (Previously Presented) An integrated circuit according to claim 19, wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

50. (Previously Presented) An integrated circuit according to claim 19, wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

51. (Previously Presented) An integrated circuit according to claim 19, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

52. (Previously Presented) An integrated circuit according to claim 19, wherein the impurity regions have dot patterns.

53. (Previously Presented) An integrated circuit according to claim 19, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

54. (Previously Presented) An integrated circuit according to claim 19, wherein a threshold voltage is controlled by controlling widths of the carrier moving regions.

55. (Previously Presented) An integrated circuit according to claim 19, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

56. (Previously Presented) The integrated circuit of claim 19 in combination with at least an electric apparatus selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

57. (New) A semiconductor device having a stacked CMOS circuit comprising:

a first layer comprising at least one first transistor;

a second layer comprising at least one second transistor over the first layer;

wherein each of the first and second transistors comprises:

a channel forming region;

a source region;

a drain region; and

a gate electrode.

58. (New) A semiconductor device having a Bi-CMOS circuit comprising:

a first layer comprising at least one bipolar transistor;

a second layer comprising at least one n-channel transistor and one p-channel transistor over the first layer;

wherein each of the n-channel transistor and the p-channel transistor comprises:

a semiconductor layer comprising:

a channel forming region;

a source region; and

a drain region;

a gate insulating film; and

a gate electrode.

59. (New) A semiconductor device having a DRAM circuit comprising:

a first layer comprising at least one capacitor comprising:

a first electrode;

a second electrode; and

an insulating film between the first and the second electrode;

a second layer comprising at least one transistor over the first layer;

wherein the transistor comprises:

a semiconductor layer comprising:

a channel forming region;

a source region; and

a drain region; and

a gate electrode.

60. (New) A semiconductor device having a SRAM circuit comprising:

a first layer comprising one first transistor;

a second layer comprising one second transistor over the first layer;

a third layer comprising one third transistor over the third layer;

wherein each of the first, second and third transistors comprises:

a channel forming region;

a source region;

a drain region;

a gate insulating film; and

a gate electrode.

61. (New) A semiconductor device having a stacked CMOS circuit comprising:

a first layer comprising at least one first transistor;

a second layer comprising at least one second transistor over the first layer;

wherein each of the first and second transistors comprises:

a channel forming region;

a source region;

a drain region; and

a gate electrode,

wherein a plurality of carrier moving regions and a plurality of impurity regions comprise an impurity element are included at least in the channel forming region.

62. (New) A semiconductor device having a Bi-CMOS circuit comprising:

a first layer comprising at least one bipolar transistor;

a second layer comprising at least one n-channel transistor and one p-channel transistor over the first layer;

wherein each of the n-channel transistor and the p-channel transistor comprises:

a semiconductor layer comprising:

a channel forming region;

a source region;

a drain region;

a gate insulating film; and

a gate electrode;

wherein a plurality of carrier moving regions and a plurality of impurity regions comprise an impurity element are included at least in the channel forming region.

63. (New) A semiconductor device having a DRAM circuit comprising:

a first layer comprising at least one capacitor comprising:

a first electrode;

a second electrode; and

an insulating film between the first and the second electrode;

a second layer comprising at least one transistor over the first layer;

wherein the transistor comprises:

a semiconductor layer comprising:

a channel forming region;

a source region; and

a drain region; and

a gate electrode;

wherein a plurality of carrier moving regions and a plurality of impurity regions comprise an impurity element are included at least in the channel forming region.

64. (New) A semiconductor device having a SRAM circuit comprising:

a first layer comprising one first transistor;

a second layer comprising one second transistor over the first layer;

a third layer comprising one third transistor over the third layer;

wherein each of the first, second and third transistors comprises:

a channel forming region;

a source region;

a drain region;

a gate insulating film; and

a gate electrode;

wherein a plurality of carrier moving regions and a plurality of impurity regions comprise an impurity element are included at least in the channel forming region.

65. (New) An electric apparatus comprising the semiconductor device according to claim 57, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

66. (New) An electric apparatus comprising the semiconductor device according to claim 58, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

67. (New) An electric apparatus comprising the semiconductor device according to claim 59, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

68. (New) An electric apparatus comprising the semiconductor device according to claim 60, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

69. (New) An electric apparatus comprising the semiconductor device according to claim 61, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car

navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

70. (New) An electric apparatus comprising the semiconductor device according to claim 62, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

71. (New) An electric apparatus comprising the semiconductor device according to claim 63, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

72. (New) An electric apparatus comprising the semiconductor device according to claim 64, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

73. (New) An EL device having the semiconductor device according to claim 57.

74. (New) An EL device having the semiconductor device according to claim 58.

75. (New) An EL device having the semiconductor device according to claim 59.

76. (New) An EL device having the semiconductor device according to claim 60.

77. (New) An EL device having the semiconductor device according to claim 61.

78. (New) An EL device having the semiconductor device according to claim 62.

79. (New) An EL device having the semiconductor device according to claim 63.

80. (New) An EL device having the semiconductor device according to claim 64.

81. (New) A semiconductor device according to claim 57, wherein the channel forming region, source region and drain region comprise single crystal silicon.

82. (New) A semiconductor device according to claim 58, wherein the semiconductor layer comprises single crystal silicon.

83. (New) A semiconductor device according to claim 59, wherein the semiconductor layer comprises single crystal silicon.

84. (New) A semiconductor device according to claim 60, wherein the channel forming region, source region and drain region comprise single crystal silicon.

85. (New) A semiconductor device according to claim 61, wherein the channel forming region, source region and drain region comprise single crystal silicon.

86. (New) A semiconductor device according to claim 62, wherein the semiconductor layer comprises single crystal silicon.

87. (New) A semiconductor device according to claim 63, wherein the semiconductor layer comprises single crystal silicon.

88. (New) A semiconductor device according to claim 64, wherein the channel forming region, source region and drain region comprise single crystal silicon.

89. (New) A semiconductor device according to claim 57, wherein the second layer has a SOI structure.

90. (New) A semiconductor device according to claim 58, wherein the second layer has a SOI structure.

91. (New) A semiconductor device according to claim 59, wherein the second layer has a SOI structure.

92. (New) A semiconductor device according to claim 60, wherein the second and third layers have a SOI structure.

93. (New) A semiconductor device according to claim 61, wherein the second layer has a SOI structure.

94. (New) A semiconductor device according to claim 62, wherein the second layer has a SOI structure.

95. (New) A semiconductor device according to claim 63, wherein the second layer has a SOI structure.

96. (New) A semiconductor device according to claim 64, wherein the second and third layers have a SOI structure.

97. (New) A semiconductor device according to claim 61, wherein the impurity element belongs to group 13.

98. (New) A semiconductor device according to claim 62, wherein the impurity element belongs to group 13.

99. (New) A semiconductor device according to claim 63, wherein the impurity element belongs to group 13.

100. (New) A semiconductor device according to claim 64, wherein the impurity element belongs to group 13.

101. (New) A semiconductor device according to claim 97, wherein the impurity element is boron.

102. (New) A semiconductor device according to claim 98, wherein the impurity element is boron.

103. (New) A semiconductor device according to claim 99, wherein the impurity element is boron.

104. (New) A semiconductor device according to claim 100, wherein the impurity element is boron.

105. (New) A semiconductor device according to claim 61, wherein the impurity element belongs to group 15.

106. (New) A semiconductor device according to claim 62, wherein the impurity element belongs to group 15.

107. (New) A semiconductor device according to claim 63, wherein the impurity element belongs to group 15.

108. (New) A semiconductor device according to claim 64, wherein the impurity element belongs to group 15.

109. (New) A semiconductor device according to claim 105, wherein the impurity element is phosphorus or arsenic.

110. (New) A semiconductor device according to claim 106, wherein the impurity element is phosphorus or arsenic.

111. (New) A semiconductor device according to claim 107, wherein the impurity element is phosphorus or arsenic.

112. (New) A semiconductor device according to claim 108, wherein the impurity element is phosphorus or arsenic.

113. (New) A semiconductor device according to claim 61, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

114. (New) A semiconductor device according to claim 62, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

115. (New) A semiconductor device according to claim 63, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

116. (New) A semiconductor device according to claim 64, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

117. (New) A semiconductor device according to claim 61, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

118. (New) A semiconductor device according to claim 62, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

119. (New) A semiconductor device according to claim 63, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

120. (New) A semiconductor device according to claim 64, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

121. (New) A semiconductor device according to claim 61, wherein the impurity regions have dot patterns.

122. (New) A semiconductor device according to claim 62, wherein the impurity regions have dot patterns.

123. (New) A semiconductor device according to claim 63, wherein the impurity regions have dot patterns.

124. (New) A semiconductor device according to claim 64, wherein the impurity regions have dot patterns.

125. (New) A semiconductor device according to claim 61, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

126. (New) A semiconductor device according to claim 62, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

127. (New) A semiconductor device according to claim 63, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

128. (New) A semiconductor device according to claim 64, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

129. (New) A semiconductor device according to claim 61, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

130. (New) A semiconductor device according to claim 62, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

131. (New) A semiconductor device according to claim 63, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

132. (New) A semiconductor device according to claim 64, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.